

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Manoj Mehrotra, et al.

Docket No: TI-32513.1

Serial No: Not Assigned

Conf. No: Not Assigned

Examiner: TBD

Art Unit: TBD

Filed: 10/22/2003

For: TRANSISTOR WITH BOTTOMWALL/SIDEWALL JUNCTION CAPACITANCE  
REDUCTION REGION AND METHOD

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

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Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on  
10-22-03.

  
Ann Trent

**PRELIMINARY AMENDMENT**

Dear Sir:

Prior to the examination of the above identified application, Applicants respectfully  
submit the following amendments and remarks.

**IN THE SPECIFICATION**

Please amend the specification by inserting before the first line the sentence:

--This application is a divisional of application Serial No. 10/253,827, filed  
September 24, 2002.--